REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and following remarks.

Applicant appreciates the indication of allowable subject matter in claims 4, 12-16 and 21-27.

By the foregoing amendment, claim 1 has been amended. Thus, claims 1-28 are currently pending in the application and subject to examination.

Claim 1 Recites Patentable Subject Matter

In the Office Action mailed December 23, 2004, claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter, "AAPA") in view of U.S. Patent No.: 6,622,010 to Ichimaru (hereinafter, "Ichimaru"). It is noted that claim 1 has been amended. To the extent that the rejections remain applicable to the claims currently pending, Applicant hereby traverses the rejections, as follows.

Independent claim 1 is directed to a PLL frequency synthesizer, which includes, among other features and advantages, a feature wherein signal flow of a feedback loop is periodically varied in a predetermined period, the predetermined period including an output period of the reference frequency signal subjected to comparison in a phase comparison cycle of the phase comparator.

Applicant respectfully submits that neither the AAPA nor Ichimaru, alone or in combination, disclose or suggest such a feature.

In the PLL frequency synthesizer of claim 1, the characteristic of the feedback loop can be varied during a period in which a pseudo correction pulse is outputted from

a charge pump circuit for each phase comparison period or cycle of a phase comparator. Accordingly, the characteristic of response of a voltage-controlled oscillator to the pseudo correction pulse outputted from the charge pump circuit can be controlled while the characteristic of the feedback loop in the steady operating state, other than the pseudo correction pulse output period set for each phase comparison cycle, is being maintained. Further, spurious generation that occurs due to the pseudo correction pulse can be suppressed in the steady operating state of the PLL frequency synthesizer.

Applicant submits that, in contrast to the claimed invention, Ichimaru discloses a frequency synthesizer provided with a divider of a fractional frequency dividing type of compensating ripple current. The fractional frequency dividing type divider is arranged to divide an oscillation signal outputted from an oscillator while periodically varying a frequency division value to generate a comparison signal, thereby changing the frequency of the oscillation signal to reduce a phase difference from a reference clock signal. Then, the frequency of the oscillation signal becomes the frequency of the reference clock signal times the average frequency division value. (*See* Ichimaru, col. 3 lines 48-53 and 61-67).

Applicant notes that in Fig. 1, after the PLL loop is locked, a timing generator 46 turns off a switching circuit 39 in a cycle of the fractional frequency division. The switching circuit 39 is turned off after the PLL loop is locked, so that a charge pump circuit 35 outputs ripple current of which the waveform is superimposed with the compensating current. (*See* col. 7, lines 10-18 and 28-33).

The output current superimposed with the compensating current can be detected directly and the current level of the compensating current can be adjusted. This makes it possible to control the current level of the compensating current based on the current level of the varying ripple current. (*See* col. 4 lines 14-22).

Thus, Applicant respectfully submits that the synthesizer of Ichimaru is designed to reduce a ripple current generated by a fractional frequency division, whereas the PLL frequency synthesizer of claim 1 is designed to suppress the pseudo correction pulse that occurs due to a signal propagation delay in the charge pump of a typical PLL frequency synthesizer including not only the fractional frequency division but also the integral frequency division.

Applicant respectfully submits that in the synthesizer of Ichimaru, the switching circuit is turned off only in the predetermined cycle of the reference clock signal within one cycle of the fractional frequency division determined by the cycle of a plurality of reference clock signals, whereas in the PLL frequency synthesizer of claim 1, the characteristic of the feedback loop is changed during a period for which the pseudo correction pulse is generated, in every cycle of the clock signal.

To qualify as prior art under 35 U.S.C. §102, a single reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, neither the AAPA nor Ichimaru, alone or combined, discloses or suggests each and every feature recited in claim 1. Specifically, neither the AAPA nor Ichimaru, alone or combined, discloses or suggests the feature "wherein signal flow of a feedback loop is periodically varied in a predetermined period, the predetermined period including an output period of

the reference frequency signal subjected to comparison in a phase comparison cycle of the phase comparator," as recited in claim 1.

For at least this reason, Applicant submits that independent claim 1 is patentably distinct over the combination of the AAPA and Ichimaru and in condition for allowance.

Claims 2-28 Recite Patentable Subject Matter

In the outstanding Office Action, claims 2-3 and 7-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Ichimaru and further in view of U.S. Patent No. 5,473,640 to Bortolini et al. (hereinafter, "Bortolini"). Claims 5-6 and 9-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of the Ichimaru, Bortolini and further in view of U.S. Patent No. 6,396,217 to Weindorf (hereinafter, "Weindorf"). Claims 11 and 17-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Ichimaru and further in view of U.S. Patent No. 5,794,130 to Abe et al. (hereinafter, "Abe"). Claims 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Ichimaru, Abe and further in view of Weindorf. Claim 28 was rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Ichimaru, Abe and further in view of U.S. Patent No. 6,226,509 to Mole et al. (hereinafter, "Mole").

Each of claims 2-28 depends from claim 1. Thus, each of claims 2-28 incorporates each and every feature of claim 1 therein. It is noted that claim 1 has been amended. To the extent that the rejections remain applicable to the claims currently pending, Applicant hereby traverses the rejections, as follows.

Independent claim 1 is directed to a PLL frequency synthesizer, which includes, among other features and advantages, a feature wherein signal flow of a feedback loop

is periodically varied in a predetermined period, the predetermined period including an output period of the reference frequency signal subjected to comparison in a phase comparison cycle of the phase comparator.

Applicant respectfully submits that none of the AAPA, Ichimaru, Bortolini, Weindorf, Abe and Mole, alone or in combination, discloses or suggests such a feature. As noted in the as noted in the Amendment of August 5, 2004, Bortolini is directed to a PLL circuit in which the PLL circuit is initialized immediately after power-up in accordance with a memory in a processor and calibration is conducted so as to shorten lock draw time immediately after the power-up. Weindorf is directed to light intensity offset error lowering method for a display lightness control device, which has a circuit for dividing voltage of DAC output. Abe is directed to a PLL circuit in which post-lock time, until the PLL circuit is locked, is shortened by changing a time constant of a filter circuit (LPF) to a time constant smaller by length of predetermined time at the time of power-on. Mole, as shown in Fig. 4, is direct to an image rejection mixer for converting frequency in which RC poly-phase filters (R1, C1-R4, C4) are arranged between transistors (Q1 through Q4) for lower input stage and transistors (Q5 through Q12) for upper mixer stage, thereby to reject image frequency components. Applicant submits that the AAPA, Ichimaru, Bortolini, Weindorf, Abe and Mole, alone or combined, do not disclose or suggest the PLL frequency synthesizer recited in claim 1.

To establish *prima facie* obviousness of a rejected claim, the applied art of record must teach or suggest each feature of a rejected claim. *See M.P.E.P. §2143.03 and In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).* As explained above, none of the AAPA, Ichimaru, Bortolini, Weindorf, Abe and Mole, alone

or in combination, discloses or suggests each and every feature of independent claim 1. Moreover, there is no suggestion to combine the references, as suggested by the Examiner in the Office Action. Accordingly, Applicant respectfully submits that independent claim 1 is neither anticipated nor rendered obvious by the cited combination, and is in condition for allowance.

Claims 2-28 depend from claim 1. Thus, claims 2-28 are allowable for the same reasons as claim 1, as well as for the additional subject matter recited therein.

Withdrawal of the rejections of claims 2-28 under 35 USC § 103(a) is respectfully requested.

CONCLUSION

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing docket number 024016-00020.

Respectfully submitted,

Arent Fox, PLLC

Michele L. Connell
Registration No. 52,763

Customer No. 004372
1050 Connecticut Ave., N.W.
Suite 400
Washington, D.C. 20036-5339
Telephone No. (202) 857-6104
Facsimile No. (202) 857-6395

MLC/sg